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# IIOT CORE / EDGE CAPTURE - LAYER 0

*Processor-resident SPA™ foundation for secure, scalable, interoperable intelligence.*

## Overview

Layer 0 serves as the **on-processor foundation** of the MIP™ Edge-to-Cloud™ continuum. It embeds **SPA™ identity**, security, and data fidelity directly within hardware execution—establishing trusted provenance at the moment of creation. As the **processor-resident origin of truth**, it provides the secure, scalable, and interoperable base on which all higher-layer intelligence operates.

## Key Features

- **Processor-Level SPA™ stamping**
- Protocol normalization across modern and legacy fieldbus for seamless interoperability
- **SecureSPA™ / QuantumSPA™ Zero-Trust encryption**
- Local **fractional historization** for resilient storage during network outages
- Containerized edge services for portable, scalable deployment in industrial environments
- **Legacy assimilation bridge**

## How it Works

- Ingests signals from machines, drives, and controllers
- Normalizes disparate protocols into a unified data fabric
- Applies **SPA™ stamps for identity and provenance**
- **Stores data locally** to minimize latency and ensure continuity
- Serves as the entry point for all higher-layer intelligence
- Lightweight loops run directly on drives/controllers

## Use Cases

- **Legacy machine integration**
- Retrofitting old PLCs under SPA™ lineage
- **Breaking vendor lock**
- Smart drive and motor monitoring with condition tracking
- Machine digital twin
- **Redundant historian**
- High-speed test bench capture for QA and validation
- Passive digital twins for non-networked assets

## Advantages

- **Preserves fidelity** by closing loops near the process
- Adds provenance without rewriting legacy code
- **Modernizes legacy systems** without replacement
- Embeds **Zero-Trust security at the processor level**
- Enables seamless multi-protocol interoperability
- Anchors immutable provenance from the first signal

L0 → L1 → L2 → L3 → L4 → L5